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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/830,378	05/29/2002	Eric Gerbault	526801-6PUS	7729

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EXAMINER	
ELMORE, JOHN E	
ART UNIT	**PAPER NUMBER**
2134	

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/830,378	GERBAULT, ERIC	
	Examiner	Art Unit	
	John Elmore	2134	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 May 2002*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5 and 8* is/are rejected.

7)☐ Claim(s) *2,3,6 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/25/2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-8 have been examined.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1, 4, 5 and 8 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Kuhn et al. ("Design Principles for Tamper-Resistant Smartcard Processors," Proceedings of the USENIX Workshop on Smartcard Technology, May 1999), hereafter Kuhn.

Regarding claim 1, Kuhn teaches an integrated circuit device containing a memory area comprised of a data memory and a program memory and wherein the memory comprises a plurality of replicas of program code, wherein said replicas reside at different addresses within said memory area, and in that said device comprises selection means for randomly selecting one replica of at least one the x blocks, as a block replica to be used when executing said program (randomized multithreading; pages 1 and 9, sections 1, 2 and 3.2).

Kuhn does not explicitly explain that the device comprises a program having N code blocks, N being an integer greater than 1, characterized in that said memory area

has M replicas, M being an integer greater than 1, of x program code blocks, x being an integer comprised between 1. Hówever, it is widely known in the art that multithreaded processing involves the simultaneous execution of different code blocks within a program. The Examiner takes official notice that the device comprises a program having N code blocks, N being an integer greater than 1, characterized in that said memory area has M replicas, M being an integer greater than 1, of x program code blocks, x being an integer comprised between 1, because one of ordinary skill in the art would recognize that for multithreaded processing a program code would be segmented into at least two code blocks, one for each thread, thus defining N as an integer greater than 1, and that there exist at least two replicas for every program code block in order to provide an alternative of addresses at each stage of operation where a code block is accessed from memory, thus defining M as an integer greater than 1.

Therefore, such a claim would be obvious to one of ordinary skill in the art at the time the invention was made for the motivation of protecting an integrated circuit device against tampering, particularly where the device is a multithreaded processor.

Regarding claim 4, Kuhn teaches all the limitations of claim 1, but does not explicitly explain that the device comprises a controller means for randomly scheduling block execution.

However, Kuhn teaches that block execution is randomly scheduled (page 9, section 3.2). The Examiner takes official notice that one of ordinary skill would recognize that a controller means is necessary to select the randomly select the blocks

to be executed and, in turn, provide the address of each selected block to a pipeline for execution.

Therefore, such a claim would be obvious to one of ordinary skill in the art at the time the invention was made for the motivation of protecting an integrated circuit device against tampering using randomized multithreading.

Regarding claims 5 and 8, this is a method version of the integrated circuit device discussed above in claims 1 and 4. Therefore, for the reasons provided above, such a claim also would have been obvious.

Allowable Subject Matter

4. **Claims 2, 3, 6 and 7 are objected to** as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 2 and 6, the closest prior art, Kuhn, does not explain that the sums of bit values of at least two addresses among the set of addresses of one replicated block and its M replicas are different. The prior art teaches only that the addresses are different, without any mention or limitation concerning how the addresses of the replicas relate to the replicated block. It would not seem obvious to one of ordinary skill to recognize such a limitation because it is not widely known in the art to

establish an addresses of a replica based on its sum to the address of the replicated block.

Regarding claims 3 and 7, the closest prior art, Kuhn, does not explain that, among the set of addresses of one replicated block and its M replicas, one address resides within the program memory and another address resides within the data memory. While the prior art teaches the use of program and data memory, the program code is accessed only from program memory. It would not seem obvious to one of ordinary skill to recognize such a limitation because it is not widely known in the art to access blocks of a program code and its replicas from both data memory and program memory, particularly where one address of a replica resides in program memory and another resides in data memory.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Elmore whose telephone number is 571-272-4224. The examiner can normally be reached on M 10-8, T-Th 9-7.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Greg Morse can be reached on 571-272-3838. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JE

David Y. Jung
Primary Examiner

8/2/05